2200001 2G Battery Management System Manual

2G ENGINEERING

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REVISION HISTORY

REV	DATE	Editor	DESCRIPTION
-	2020-02-14	JL	Initial Release
A	2020-05-14	JL	Corrected documentation on passive mode
B	2020-06-22	JL	Updated INTERNAL_STATE bits. Updated SYSTEM_FAULTS bits. Revamped product definition section, including description of all parameters in product definition .ini file.
C	2020-07-08	JL	Updated fault bits
D	2020-10-08	JL	Added DRAIN_V and DRAIN_EN registers
E	2020-10-16	JL	Added DISCHG_BLIP, XDCR_UNITS, INTERLOCK_FILT_C, and XDCR_POWER registers. Updated bits in MONITOR_PASS and MONITOR_FAIL fields.
F	2021-04-22	JL	Added emergency reset sequence. Updated “Communicating with the BMS” section
G	2021-06-03	JL	Added FAULT_RST_TIMEOUT register
H	2023-05-08	JL	Updated date formatting in document. Added AUX_CH_ENABLE, EXT_ADC, CS, EXT_DI, AUX_CH_DIGITAL_STATE, AUX_CH_x_OUT_SETUP, AUX_CH_x_THRESHOLD, AUX_CH_x_SOURCE, AUX_THERMO_CTRL_COLD, and AUX_THERMO_CTRL_HOT registers
J	2025-01-07	JL	Added DISPLAY_MODE register. Updated AUX_CH_x_SOURCE registers.
K	2025-04-30	JL	Added additional product definition parameters. Added extended cell voltage/temperature registers. Added note on actual safety parameter reporting.
L	2025-06-11	JL	Added WATER_ALARM_m_n register
M	2026-01-06	JL	Added XDCR2_UNITS, XDCR3_UNITS, XDCR_GAIN, XDCR2_GAIN, XDCR3_GAIN, XDCR_OFFSET, XDCR2_OFFSET, XDCR3_OFFSET, ACTV_WHILE_CHARGING, RS485_TERM_IN_PASSIVE, COMMS_PHY, DATA_LOG_TRIG_MASK registers. Added

			new fault bits in SYSTEM_FAULTS register. Added new bits to MONITOR_PASS/MONITOR_FAIL sections. Added new bit to INTERNAL_STATE register. Added Data Logging section. Added use_dynamic_i_chg_limit to Product Definition Parameters section. Added Dynamic Current Limiting section.
N	2026-02-06	JL	Added Dynamic Discharge Limiting section. Added dynamic discharge current limit bit to INTERNAL_STATE register. Added use_dynamic_i_dischg_limit parameter to Product Definition Parameters section. Added dynamic discharge configuration fault bit to SYSTEM_FAULTS register. Added notes about range of CHG_I_LIMIT_REQ/DISCHG_I_LIMIT_REQ registers to their respective sections.

Description

2G BMS Operation

The 2G BMS is intended to be integrated into a battery pack. It provides protection for overcurrent, overcharge, and undercharge; provides cell balancing; and tracks battery information such as voltage, current, and state of charge.

Specifications

Battery Pack voltage	8.4V to 400+V (depending on configuration)
Cell Count	2 to 100 (depending on configuration)
Communications Protocol	MODBUS RTU/ASCII/TCP, HTTP
Host Communications Interfaces	RS-232, RS-485, Ethernet
Operating Environment	PBOF -20C to 55C
Standby power draw	< 0.5 mA
Onboard flash memory size	32MB
Default Baud Rate	115200
Default Modbus Address	1

Hardware

Connectors & Pinouts

See GA drawing for details on specific models.

Power Modes

The battery has 4 power modes which are automatically entered based on system conditions.

Active Mode

In active mode, the BMS is actively monitoring the state of the battery cells. Modbus communications with the battery are available. Battery charge and discharge are supported. The BMS can leave active mode and enter passive mode based on lack of communications, lack of wakeup assertion, both, or neither. From active mode, the BMS can also be commanded into the sleep or hibernate state via Modbus. For easy identification of this state, the BMS' heartbeat LED will flash at 2Hz when in active mode.

Passive Mode

In passive mode, the BMS is actively monitoring the state of the battery cells. Modbus communications with the BMS are not available. Battery charge and discharge are supported. The BMS can be returned to active mode by asserting the wakeup line. This mode significantly reduces quiescent power, allowing the battery to last longer in low-power use cases. For easy identification of this state, the BMS' heartbeat LED will flash at 0.5Hz when in passive mode. If the BMS is equipped with a display, it will be disabled in this state.

Sleep Mode

In sleep mode, most of the BMS' internal electronics are powered down. Modbus communications are unavailable. Battery charge and discharge are unavailable. In this mode, the BMS will only check battery conditions once every 10 minutes instead of continuously. This mode can be manually entered via Modbus command for storage of the battery, or will be automatically entered once the battery cells reach a cutoff voltage. The BMS will leave sleep mode within 10 minutes if it detects the presence of an external charger. The BMS can also be taken out of sleep mode using the wakeup signal. If the battery cells are at a safe voltage, the BMS will return to active mode immediately upon assertion of the wakeup signal. If the battery cells are not at a safe voltage, an external charger must be present for the battery to remain in active mode when the wakeup signal is asserted.

If the BMS is left in sleep mode for an extended period of time, the battery cells will continue to slowly discharge. Eventually, they will discharge below a critical threshold and the system will switch to hibernate mode, if supported by the BMS.

If hibernate mode is not supported on the BMS, it is recommended to check the status of the battery every 6 months when in storage.

Hibernate Mode

Note: Not all BMS variants support hibernate mode.

In hibernate mode, all of the BMS' internal electronics are powered down. Modbus communications are unavailable. Battery charge and discharge are unavailable. If hibernate mode was entered via a Modbus command, the system can be returned to active mode by asserting the wakeup signal. If hibernate mode was entered due to low battery voltage, an external battery charger must be connected while asserting wakeup in order to return the BMS to active mode.

Communicating with the BMS

By default, the BMS can communicate with a host system over RS-232, RS-485, or Ethernet, depending on equipped interfaces. The default mode for serial communications is Modbus RTU at address 1 with baud rate 115200, 8N1. 2G Engineering's JAMBUI software is the suggested software for battery communication with a PC.

When connecting via Ethernet, up to 6 clients can be connected to the battery via Modbus TCP on port 502.

A basic web interface for the battery is also available on port 80.

Charging/Discharging the battery

The BMS contains two MOSFET switches which control power flow in to and out of the battery. These switches are referred to as the charge and discharge switches, respectively. The discharge switch is controlled by a combination of a user request register (PACK_DISCHG) and various system safety checks. The charge switch is always enabled unless system conditions disable it. The default state of the discharge switch (after initial pack installation, sleep, and hibernate) can be configured using the DEFAULT_DISCHG_STATE register. The actual states of the charge and discharge switches may differ from the expected states due to system safety protections. The actual states of the switches can be checked using the PACK_CHG_ACTUAL and PACK_DISCHG_ACTUAL registers. The reason for the difference can then be determined by looking at the SYSTEM_STATE register.

The battery can be charged by either a constant current/constant voltage (CC/CV) charger or a constant current (CC) only charger. Charging is stopped (by disabling the charge switch) when the cell voltages exceed their cutoff voltages. With a CC/CV charger, this should occur when the pack is fully charged. When using a CC charger, this may occur before the pack has fully charged. To allow the pack to finish charging, the system will automatically re-enable charging after a pre-programmed amount of time has elapsed. Charging can also be resumed immediately by writing 1 to the PACK_CHG register.

Balancing

The system includes a built-in balancing circuit to ensure that all cells in the pack stay matched in voltage. Balancing is automatically enabled when the battery is charging, and is applied to any cells which are at a voltage sufficiently above the minimum cell in the pack. When charging concludes, any cells which were balancing at that time will continue balancing until they are matched to the rest of the pack. A balance cycle can be started at any time by writing a 1 to the BALANCE_STATE register, and can be cancelled by writing 0 to the BALANCE_STATE register.

Safety

The BMS has a number of safety features which protect both the battery and the user under various fault conditions. These conditions include:

- Over current and Short Circuit
- Over voltage on cells
- Under voltage on cells
- Over temperature on cells during charge and discharge
- Under temperature on cells during charge and discharge
- Over temperature on internal MOSFETs
- Over temperature on main control board

The limits for these protection features are set at the factory, but can be viewed by looking at the product configuration registers. Due to hardware resolution limits, the requested values may not always exactly match the actual values which are in effect. Beginning with firmware version 1.17, the actual, rather than requested, values will be reported in the corresponding Modbus registers.

For the over current protection while discharging, an automatic retry feature is available that will attempt to reconnect re-enable the battery a specified number of times after a specified interval has elapsed. See the FAULT_RETRY_COUNT and FAULT_RETRY_INTERVAL configuration registers for more information.

If an overcurrent event occurs while charging, the system will disable charging until a 1 is written to the PACK_CHG register.

Configuration Registers

All registers in this group are temporary unless saved by writing 1 to the WRITE_CONFIG register.

COM_PASSIVE_TIMEOUT

Sets the interval that must elapse without communications in order for the battery to enter passive mode. If set to 0, lack of communications will not be considered when deciding to enter passive mode.

WAKE_PASSIVE_TIMEOUT

Sets the interval that must elapse without assertion of the wakeup line in order for the battery to enter passive mode. If set to 0, the wakeup line will not be considered when deciding to enter passive mode. If COM_PASSIVE_TIMEOUT is also zero, the system will never enter passive mode. If both COM_PASSIVE_TIMEOUT and WAKE_PASSIVE_TIMEOUT are nonzero, both conditions must be satisfied before the system can enter passive mode.

FAULT_RETRY_COUNT

Specifies the number of times the BMS will re-enable the battery output after it has been disabled due to an overcurrent condition. If set to 0, the BMS will retry forever.

FAULT_RETRY_INTERVAL

Specifies the interval between retries after an overcurrent cutoff. If set to 0, the BMS will never retry and the output will need to be re-enabled manually via Modbus command.

DEFAULT_DISCHG_STATE

Specifies the discharge output state of the battery after waking up from sleep or hibernate mode.

0. Always off
1. Always on
2. Use last user-commanded state

MODBUS_ADDR

Specifies the Modbus address that the BMS will respond to. This takes effect immediately, so you will need to specify the new address in your software as soon as this register has been written.

MODBUS_MODE

Specifies the modbus mode that the BMS will operate in. This takes effect immediately, so you will need to specify the new mode in your software as soon as this register has been written.

0. RTU
1. ASCII

SERIAL_BAUD

Specifies the baud rate used for serial communications with the BMS. This takes effect immediately, so you will need to specify the new baud rate in your software as soon as this register has been written.

IP_CONFIG

Specifies configuration options related to IP communications.

Bit 0: 0 = Use static IP, 1 = Use DHCP

IPV4_ADDR

If static IP mode is selected, this register specifies the static IP.

IPV4_MASK

If static IP mode is selected, this register specifies the subnet mask.

IPV4_GW

If static IP mode is selected, this register specifies the default gateway.

INTERLOCK_MODE

If the BMS is equipped with an external interlock input, this register controls its operation. Available interlock modes are listed below.

0. Interlock disabled. The interlock pin will have no effect on system operation.
1. Interlock enabled. The discharge switch will only be allowed to turn on if the voltage on the interlock is between INTERLOCK_MIN_V and INTERLOCK_MAX_V.

INTERLOCK_MIN_V

The minimum voltage, above which the interlock will enable the discharge output.

INTERLOCK_MAX_V

The maximum voltage, below which the interlock will enable the discharge output.

XDCR_UNITS, XDCR2_UNITS, XDCR3_UNITS

(Only in firmware version ≥ 1.7) Allows setting the display units for the corresponding transducer input to a user-defined string. Not all systems will support all inputs. The default value for the first and second transducer is “Bar”. The default value for the third transducer is “%”.

INTERLOCK_FILT_C

(Only in firmware version ≥ 1.7) Allows configuration of the constant α used for filtering of the interlock voltage. The interlock voltage is filtered using the following formula:

$$V = (\alpha \times V_{current}) + \left((1.0 - \alpha) * V_{last}\right)$$

A value of 1.0 for the filtering constant therefore provides no filtering. The amount of filtering is increased as the filtering constant is decreased towards zero.

XDCR_GAIN, XDCR2_GAIN, XDCR3_GAIN

Sets the gain applied to the corresponding transducer input voltage.

XDCR_OFFSET, XDCR2_OFFSET, XDCR3_OFFSET

Sets the offset applied to the corresponding transducer input value. Offset is applied after gain.

FAULT_RST_TIMEOUT

(Only in firmware version ≥ 1.9) Allows configuration of discharge overcurrent fault auto-reset time interval. If set to 0, this feature is disabled. When enabled, this feature will automatically reset the internal overcurrent fault counter after the battery's discharge switch has been on continuously for more than the amount of time specified in this register. This can be used, for example, to allow a finite number of overcurrent fault retries during system startup, while also allowing the same number of overcurrent fault retries during system operation if a genuine fault condition occurs.

The timer used for this feature is started every time the discharge switch transitions from the off state to the on state. Note that the discharge switch may be turned on automatically under certain conditions when the battery is charging. This may result in the fault counter being reset during charging. Given the intended usage of this feature, this is not expected to be a problem.

AUX_CH_x_OUT_SETUP (x = 1 to 8)

On units equipped with digital outputs, these registers configure the behavior of the corresponding output. This is a composite register with the following fields:

Mode

Configures the operating mode of the digital output. The following values are supported:

0. Digital. Output pin is set to high value when active, low value when inactive.
1. PWM. Output pin is set to a specified PWM duty cycle when active, low value when inactive.
2. Peak & Hold PWM. When activated, the output pin will be set to the peak duty cycle for the peak time, then the hold duty cycle for the hold time. If the peak time is set to 0, only the hold duty cycle will be considered. If the hold time is nonzero, the peak/hold cycle will be repeated when the hold time expires. The peak/hold cycle will repeat indefinitely as long as the output is activated.
3. Thermo Control – Cold. Output pin is set to a high value when triggered based on the conditions in the AUX_THERMO_CTRL_COLD register. Unimplemented in current firmware.
4. Thermo Control – Hot. Output pin is set to a high value when triggered based on the conditions in the AUX_THERMO_CTRL_HOT register. Unimplemented in current firmware.

Peak Time

In peak & hold PWM mode, configures the amount of time the output spends in the peak duty cycle state when triggered. If set to 0, the peak phase is skipped. Value in milliseconds. Current firmware has a resolution of 100ms.

Hold Time

In peak & hold PWM mode, configures the amount of time the output spends in the hold duty cycle state when triggered. If set to 0, the output will remain in the hold state as long as the output is triggered. Otherwise, it will return to the peak state and the peak/hold cycle will repeat as long as the output is triggered. Value in milliseconds. Current firmware has a resolution of 100ms.

Peak Duty Cycle

In PWM mode, configures the static duty cycle which will be used when the output is triggered. In peak & hold PWM mode, configures the duty cycle which will be used when in the peak state. Value in percent.

Hold Duty Cycle

In peak & hold PWM mode, configures the duty cycle which will be used when in the hold state. Value in percent.

PWM Frequency

Configures the PWM frequency used for the output when in a PWM mode. Value in Hz.

AUX_CH_x_THRESHOLD (x = 1 to 8)

On units equipped with analog inputs, these registers configure the limits used when the analog inputs are read as digital inputs or used to trigger output changes. This is a composite register with the following fields:

Inverted

The following values are supported:

0. The analog input will be considered to have a true value if between the low threshold and the high threshold, and a false value otherwise.
1. The analog input will be considered to have a false value if between the low threshold and the high threshold, and a true value otherwise.

Low Threshold

Low comparison value for the analog input. Must be less than the high threshold value. Value in volts.

High Threshold

High comparison value for the analog input. Must be greater than the low threshold value. Value in volts.

AUX_CH_x_SOURCE (x = 1 to 8)

On units equipped with digital outputs, these registers configure trigger sources which can change the state of the corresponding output. This is a composite register with the following fields:

Source Control Enable

The following values are supported:

0. Output channel is not controlled by configured trigger sources.

1. Output channel is controlled by configured trigger sources.

Inverted

The following values are supported:

0. The configured trigger source value is passed directly to the output pin.
1. The configured trigger source value is logically inverted before being passed to the output pin.

Logic Operand

The following values are supported:

0. AND. All of the trigger sources specified in the source bit mask must be true in order for the trigger value to be considered true.
1. OR. Any of the trigger sources specified in the source bit mask must be true in order for the trigger value to be considered true.

Source Bit Mask

Configures which trigger sources are enabled for this channel. Setting the bit in the corresponding position enables the source. The following sources are defined:

0. Interlock input. Considered true when the voltage on the interlock pin is between INTERLOCK_MIN_V and INTERLOCK_MAX_V.
1. Wakeup input.
2. Analog input 1. Values in AUX_CH_1_THRESHOLD are used to determine the digital value.
3. Analog input 2. Values in AUX_CH_2_THRESHOLD are used to determine the digital value.
4. Analog input 3. Values in AUX_CH_3_THRESHOLD are used to determine the digital value.
5. Analog input 4. Values in AUX_CH_4_THRESHOLD are used to determine the digital value.
6. Reserved.
7. Reserved.
8. Reserved.
9. Reserved.
10. Reserved.
11. Reserved.
12. Reserved.
13. Reserved.
14. Loss of comms. The trigger source is activated whenever bit 14 is set in the ERR/SYSTEM_FAULTS registers. Only available on firmware version 1.15 or later.

AUX_THERMO_CTRL_COLD

Configures the temperature control mode for cold temperatures. This function is unsupported in the current firmware release. This is a composite register with the following fields:

Mode

The following values are supported:

0. Always On. The control mode is active at all times.

1. Only while charging. The control mode is only active when the battery is charging. At other times, it is always considered to have a false value.

On Temp

Temperature below which the trigger source activates. Value in degrees C.

Off Temp

Temperature above which the trigger source deactivates. Must be greater than or equal to the on temp. Value in degrees C.

AUX_THERMO_CTRL_HOT

Configures the temperature control mode for hot temperatures. This function is unsupported in the current firmware release. This is a composite register with the following fields:

Mode

The following values are supported:

0. Always On. The control mode is active at all times.
1. Only while charging. The control mode is only active when the battery is charging. At other times, it is always considered to have a false value.

On Temp

Temperature above which the trigger source activates. Value in degrees C.

Off Temp

Temperature below which the trigger source deactivates. Must be less than or equal to the on temp. Value in degrees C.

ACTV_WHILE_CHARGING

If set to 1, the BMS will remain in active mode while the battery is charging. If set to 0, the BMS will enter passive mode while charging according to its configured power management settings.

RS485_TERM_IN_PASSIVE

If the BMS is equipped with a switchable communications termination resistor, it will normally be turned off when this register is set to 0 and the system enters passive mode. If you need the termination resistor to stay enabled when the system enters passive mode (e.g. to provide termination for other devices on the bus), set this register to 1.

COMMS_PHY

On some systems, multiple communications physical layers are available on the same external pins. The active physical layer can be selected by writing to this register. The following values may be supported, depending on the specific BMS model:

0. RS-232
1. RS-485
2. CAN bus

DATA_LOG_TRIG_MASK

Configures which SYSTEM_FAULT bits will trigger a data log event when they are set. A bit set in this register means that the corresponding bit in SYSTEM_FAULTS will serve as a log trigger. See the SYSTEM_FAULTS register for more information on the available faults, and the Data Logging section of this manual for more information on the data logging system.

Control Registers

These registers are used to control the current state of the BMS.

BATT_POWER_STATE

Write 1 to put the BMS into sleep mode. The BMS will stay asleep until wakeup is asserted or an unsafe battery cell condition is detected.

PACK_CHG

Charging is always enabled unless system conditions prevent it. If the actual state of the charge switch is off due to hysteresis on over voltage or an over current event, writing 1 to this will reset the hysteresis for over voltage detection. The charge switch will immediately turn off again if system conditions are still unsafe.

PACK_DISCHG

Write 1 to enable discharging the battery. Write 0 to disable discharging the battery. If the actual state of the discharge switch is off due to hysteresis on under voltage, writing 1 to this will reset the hysteresis on under voltage detection. The discharge switch will immediately turn off again if system conditions are still unsafe.

BALANCE_STATE

This will read 1 if any cells are currently balancing. Write 1 to force a balance cycle. Write 0 to cancel balancing for all actively-balancing cells. Balancing may be immediately re-enabled if cell conditions dictate.

DRAIN_V

(Only in firmware version ≥ 1.6) This register sets the cell voltage to which the pack should be drained in forced discharge mode. This register is volatile and will reset to 0 if the system enters sleep or hibernate mode.

DRAIN_EN

(Only in firmware version ≥ 1.6) Write 1 to enable forced discharge mode. Write any other value to cancel forced discharge mode. Forced discharge mode will be automatically cancelled if any of the following conditions are met:

- DRAIN_V is set to a value less than or equal to 0
- DRAIN_V is set to a value less than PROD_VMIN_CELL or PROD_VMIN_BALANCE
- All cell voltages are less than DRAIN_V
- The system enters sleep or hibernate mode

Once forced discharge mode has been cancelled for any reason, it will not be automatically re-enabled. The user must write 1 to DRAIN_EN to begin force-discharging the battery again.

DISCHG_BLIP

(Only in firmware version ≥ 1.7) Writing a time interval (in seconds) to this field will temporarily disable the discharge output switch of the battery for that amount of time. Once the time expires, the discharge switch will be re-enabled. If the discharge switch is already disabled, this register will have no effect. Reading this register will return the amount of time remaining before the discharge switch is re-enabled. Writing 0 to this register at any time will return the battery to normal operation.

XDCR_POWER

Controls power to the internal pressure transducer(s). In firmware versions ≥ 1.7, this value is persistent. In previous firmware versions, it will be reset every time the battery enters sleep or hibernate mode.

DISPLAY_MODE

(Only in firmware version ≥ 1.15) Configures which statuses are shown on the internal display, if equipped. The following statuses will be shown if the corresponding bit is set in this register.

0. Pack voltage
1. State of charge
2. IP Address
3. Transducer 1 value
4. Transducer 2 value
5. Transducer 3 value
6. Pack current
7. Minimum cell temp
8. Maximum cell temp
9. Average cell temp
10. Minimum MOSFET temp
11. Maximum MOSFET temp
12. Average MOSFET temp
13. Minimum board temp
14. Maximum board temp
15. Average board temp
16. Minimum cell voltage
17. Maximum cell voltage
18. Average cell voltage
19. Analog Input 1
20. Analog Input 2
21. Analog Input 3
22. Analog Input 4

Battery Status Registers

These registers report information about the current state of the BMS and attached battery cells.

ERR

This register mirrors the lower 16 bits of the SYSTEM_FAULTS register.

SYSTEM_FAULTS

This register returns a bit field where each bit is set to 1 in the event of a specific system failure. These bits can be written in order to clear them. Writing 65535 to this register will request a soft reset of the system. The bits used in this register are defined below. These bits are correct for firmware versions ≥ 1.5.

0. Product definition is invalid or failed to load
1. Reserved
2. Internal file system failure
3. A battery cell under voltage condition has occurred
4. A battery cell over voltage condition has occurred
5. Firmware upgrade failure
6. A battery over temperature condition has occurred for charging
7. A battery under temperature condition has occurred for charging
8. A battery over temperature condition has occurred for discharging
9. A battery under temperature condition has occurred for discharging
10. A FET over temperature condition has occurred
11. A control board over temperature condition has occurred
12. An over current condition has occurred while discharging
13. Set when the system has been soft reset or taken out of sleep/hibernate modes
14. Modbus communications with host have timed out
15. Incorrect parameter supplied to modbus command or general software error
16. Configuration storage failure – default configuration options may have been loaded
17. Battery pack is currently unbalanced
18. State of charge measurement failure – reported state of charge may be inaccurate until the battery has been fully recharged
19. Battery monitoring IC failure
20. Battery product definition contains invalid values
21. Voltage correction subsystem failure
22. Dynamic charge limit data file is invalid or incorrectly formatted
23. Dynamic discharge limit data file is invalid or incorrectly formatted
24. An over current condition has occurred while charging

PACK_V

The voltage of the battery pack.

BAT_I

The current entering or leaving the battery pack. Negative current represents discharging and positive current represents charging.

BAT_AH

The number of amp-hours that have been pulled out of the battery since the last full charge.

BAT_NET_AH

The remaining number of amp-hours in the battery based on the programmed pack size.

SOC

The current state of charge estimate of the battery pack.

CELL_V, CELL_V_m_n

A list of the voltages on each cell in the battery pack. The CELL_V register will only show the first 15 cell voltages. Firmware 1.16 and later support systems with higher cell counts. The remaining cell voltages are reported in the CELL_V_m_n registers, e.g. the first 30 cell voltages are accessible in the CELL_V_1_30 register, the next 30 cell voltages are accessible in the CELL_V_31_60 register, and so on.

CELL_COUNT

The number of cells in the battery pack.

TS_COUNT

The number of temperature sensors in the system.

TEMPS, TEMPS_m_n

A list of the temperatures reported by all temperature sensors in the system. The assignment of various temperature sensors in the system is indicated by the PROD_CELL_T_BITS, PROD_FET_T_BITS, and PROD_BOARD_T_BITS registers. On systems with higher temperature sensor counts, the complete set of temperatures can be accessed in the TEMPS_m_n registers. For example, the first 30 temperature sensors are accessible in the TEMPS_1_30 register, the next 30 temperature sensors are accessible in the TEMPS_31_60 register, and so on. See the GA drawing for details on temperature sensor ordering on your specific BMS product.

MIN_CELL_V

The voltage of the lowest cell in the pack.

MAX_CELL_V

The voltage of the highest cell in the pack.

AVG_CELL_V

The average voltage of all cells in the pack.

MIN_CELL_T

The minimum temperature among all battery cell temperature sensors present in the BMS.

MAX_CELL _T

The maximum temperature among all battery cell temperature sensors present in the BMS.

AVG_CELL_T

The maximum temperature among all battery cell temperature sensors present in the BMS.

MIN_FET_T

If the BMS is equipped with internal FET temperature sensors, this register reports the lowest temperature among all FET temperature sensors.

MAX_FET_T

If the BMS is equipped with internal FET temperature sensors, this register reports the highest temperature among all FET temperature sensors.

AVG_FET_T

If the BMS is equipped with internal FET temperature sensors, this register reports the average temperature among all FET temperature sensors.

MIN_BOARD_T

The minimum temperature among all control board temperature sensors present in the BMS.

MAX_BOARD_T

The maximum temperature among all control board temperature sensors present in the BMS.

AVG_BOARD_T

The maximum temperature among all control board temperature sensors present in the BMS.

PACK_CHG_ACTUAL

The actual state of the pack charge switch. This may differ from the expected state for a variety of reasons. See the INTERNAL_STATE register.

PACK_DISCHG_ACTUAL

The actual state of the pack discharge switch. This may differ from the requested state for a variety of reasons. See the INTERNAL_STATE register.

PACK_CHARGING

Reads 1 if the system currently believes the battery pack is charging.

BALANCE_BITS, BALANCE_BITS_m_n

A bit will be set for each cell that is currently in a balancing state. The BALANCE_BITS register will only indicate the balance state for the first 16 cells. On systems with higher cell counts, the complete set of cell balancing bits can be accessed in the BALANCE_BITS_m_n registers. For example, the balance bits for the first 300 cells in the system can be accessed in the BALANCE_BITS_1_300 register.

BATTERY_FULL

Reads 1 if the system has completed a full charge and is at greater than 99% state of charge.

INTERNAL_STATE

A set of bits which indicate the state of the internal battery safety system. This register will generally indicate the reason that the actual state of the charge/discharge switches disagrees with the requested state.

0. Charge switch is disabled due to over temperature condition or hysteresis on over temperature condition
1. Charge switch is disabled due to under temperature condition or hysteresis on under temperature condition
2. Discharge switch is disabled due to over temperature condition or hysteresis on over temperature condition
3. Discharge switch is disabled due to under temperature condition or hysteresis on under temperature condition
4. Charge switch is disabled due to over voltage condition or hysteresis on over voltage condition
5. Discharge switch is disabled due to under voltage condition or hysteresis on under voltage condition
6. Discharge switch is disabled due to over current condition
7. Charge switch is disabled due to over current condition
8. Charge/Discharge switches are disabled due to FET over temperature condition
9. Charge/Discharge switches are disabled due to control board over temperature condition
10. Discharge switch is disabled due to external interlock input
11. Discharge switch is in a cooldown period after switching
12. Charge switch is in a cooldown period after switching
13. Charge switch is disabled due to dynamic over current condition
14. Discharge switch is disabled due to dynamic over current condition

WATER_ALARM, WATER_ALARM_m_n

If the BMS is equipped with a water alarm, this register returns a value between 0% and 100%, where 0 is no conductivity, and 100% is a dead short across the water alarm contacts. A value greater than 1% is generally cause for concern. On systems with more than one independent water alarm sensor, the complete set of water alarm sensors can be accessed in the WATER_ALARM_m_n register. For example, the first 30 water alarm sensor values can be accessed in the WATER_ALARM_1_30 register.

INTERLOCK_V

If the BMS is equipped with an external interlock pin, this register will return the voltage on the external interlock.

AUX_ADC1

If the BMS is equipped with an auxiliary ADC input, this register will return the voltage on that input.

MONITOR_PASS / MONITOR_FAIL

These registers are bit fields which indicate that certain subsystems of the BMS are or are not functioning normally. The pass bit will be set when the system has evidence that the subsystem is working correctly, and the fail bit will be set when the system has evidence that the subsystem is not working correctly. This means that both bits can be set if the subsystem transitions between a working and non-working state, or neither bit may be set if the state of the subsystem has not yet been determined. The MONITOR bits are defined below.

0. Internal Flash memory
1. Stored configuration data
2. Internal file system
3. Product definition
4. Persistent data (including state of charge)
5. Internal power management
6. Watchdog timer
7. Reserved
8. Reserved
9. Reserved
10. Reserved
11. Reserved
12. Reserved
13. Reserved
14. Reserved
15. Reserved
16. Reserved
17. Reserved
18. Reserved
19. Battery monitoring
20. Battery reference calibration
21. Real-time clock
22. Ethernet MAC address
23. Ethernet
24. Digital control board temperature sensor
25. LED display (Only in firmware version ≥ 1.7)
26. Voltage correction
27. Dynamic charge current limit configuration
28. Reserved
29. Reserved
30. Reserved
31. System Initialization

AUX_CH_ENABLE

If the BMS is equipped with digital outputs, this register reports the triggered status of each pin.

EXT_ADC

If the BMS is equipped with external analog inputs, this register will report the voltage on each external analog input. Unavailable inputs will report as NaN.

CS

If the BMS is equipped with digital outputs, this register will report the current being driven out of each output pin. Outputs which do not support current sensing will report as NaN.

EXT_DI

If the BMS is equipped with digital inputs, this register will report the value of the digital input pins. The state of each pin will be reflected in the corresponding bit in this register. Note that on some hardware configurations, the digital and analog inputs may share the same physical pins.

AUX_CH_DIGITAL_STATE

If the BMS is equipped with external analog inputs, this register will report the state of each analog input as a digital value. The analog limits used for conversion to digital are configured in the AUX_CH_x_THRESHOLD registers. The state of each pin will be reflected in the corresponding bit in this register.

Product Definition File

The product definition is used by the factory to configure various fixed aspects of the BMS. Some of the parameters are exposed in read-only format via Modbus for convenience. In general, these parameters are not intended to be user-configurable. Misconfiguration of these parameters can cause serious damage to the BMS and may create a fire and/or explosion risk.

If instructed to modify the product definition file, it is located in the BMS's file system at /cfg/prod.ini. A backup copy is located at /cfg/prod.bak. When updating the product definition file, both the primary and backup files should be updated at the same time to ensure consistency.

The product definition parameters, along with their corresponding Modbus registers, are listed in the following section.

Product Definition Parameters

[product] section

Parameter name	Modbus register name	Description
version	PROD_VERS	Product definition file version. Used internally, should not be changed.
cellcount	CELL_COUNT	Number of cells supported by the BMS. Hardware-dependent, should not be changed.
tscount_internal	-	Number of temperature sensors on internal ADC channels. Hardware-dependent, should not be changed.

tscount_external	-	Number of temperature sensors on external ADC channels. Hardware-dependent, should not be changed.
bms_ic	PROD_BMS_IC	Model identifier for monitoring IC. Hardware-dependent, should not be changed.
r_sense	PROD_R_SENSE	Internal current sense resistor value, in µOhm. Hardware-dependent, should not be changed.
quiescent_current_active	PROD_IQ_ACTV	Current sense offset in active mode.
quiescent_current_passive	PROD_IQ_PASV	Current sense offset in passive mode.
quiescent_current_sleep	PROD_IQ_SLEEP	Current sense offset in sleep mode.

[batt] section

Parameter name	Modbus register name	Description
capacity_ah	PROD_PACK_CAPACITY	Capacity of the battery pack in amp-hours.
balance_deviation_v	PROD_BAL_DEV	Voltage above the lowest cell voltage required for any other cell to balance.
vmax_cell	PROD_VMAX_CELL	Hardware charge cutoff voltage. This is a failsafe cutoff only; under normal circumstances charging should be stopped by other limits before it gets to this point.
vmin_cell	PROD_VMIN_CELL	Hardware discharge cutoff voltage. This is a failsafe cutoff only; under normal circumstances discharging should be stopped by other limits before it gets to this point. If a cell voltage falls below this voltage, balancing will be disabled for that cell.
min_balance_voltage	PROD_VMIN_BALANCE	If a cell voltage falls below this voltage, balancing will be disabled for that cell.
balance_hysteresis	PROD_BALANCE_HYST	If a cell voltage falls rises above (min_balance_voltage + balance_hysteresis), balancing will be allowed for that cell.
tmax_charge	PROD_TMAX_CHG	If any cell temperature exceeds this temperature, charging will be disabled.

tmin_charge	PROD_TMIN_CHG	If any cell temperature falls below this temperature, charging will be disabled.
tcharge_hysteresis	PROD_TCHG_HYST	Hysteresis on cell charging temperature limits. If all cell temperatures fall below (tmax_charge – tcharge_hysteresis) or rise above (tmin_charge + tcharge_hysteressis), charging will be re-enabled if it had previously been disabled due to cell temperature.
tmax_discharge	PROD_TMAX_DISCHG	If any cell temperature senor exceeds this temperature, charging will be disabled.
tmin_discharge	PROD_TMIN_DISCHG	If any cell temperature senor falls below this temperature, charging will be disabled.
tdischarge_hysteresis	PROD_TDISCHG_HYST	Hysteresis on cell discharging temperature limits. If all cell temperatures fall below (tmax_discharge – tdischarge_hysteresis) or rise above (tmin_discharge + tdischarge_hysteressis), discharging will be re-enabled if it had been disabled due to cell temperature.
tmax_fet	PROD_TMAX_FET	If any FET temperature senor exceeds this temperature, charging and discharging will be disabled.
tfet_hysteresis	PROD_TFET_HYST	Hysteresis on FET temperature limit. If all FET temperatures fall below (tmax_fet – tfet_hysteresis), charging and discharging will be enabled if they had been disabled due to FET temperature.
tmax_board	PROD_TMAX_BOARD	If any board temperature senor exceeds this temperature, charging and discharging will be disabled.
tboard_hysteresis	PROD_TBOARD_HYST	Hysteresis on board temperature limit. If all board temperatures fall below (tmax_fet – tfet_hysteresis), charging and discharging will be enabled if they had been disabled due to board temperature.

vmax_charge	PROD_VMAX_CHG	Cell cutoff voltage for charging. If any cell exceeds this voltage, charging will be disabled and the state of charge counter will be reset. This parameter is particularly relevant when using a constant-current-only charger.
vcharge_hysteresis	PROD_VCHG_HYST	Hysteresis on cell charge cutoff voltage. If every cell falls below (vmax_charge – vcharge_hysteresis), charging will be re-enabled if it had been disabled due to cell voltage.
vmin_discharge	PROD_VMIN_DISCHG	Cell cutoff voltage for discharging. If any cell falls below this voltage, discharging will be disabled.
vdischarge_hysteresis	PROD_VDISCHG_HYST	Hysteresis on cell discharge cutoff voltage. If every cell voltage exceeds (vmin_discharge + vdischarge_hysteresis), discharging will be re-enabled if it had been disabled due to cell voltage.
imax_fet_discharge	PROD_IMAX_FET_DISCHG	If charge current exceeds this value, the discharge FET will be forced on to take stress off the body diode.
imax_fet_charge	PROD_IMAX_FET_CHG	If discharge current exceeds this value, the charge FET will be forced on to take stress off the body diode.
charge_reset_time	PROD_CHG_RESET_TIME	If charging was disabled due to a cell voltage exceeding vmax_charge, but the maximum cell voltage has not fallen below (vmax_charge – vcharge_hysteresis), charging will be re-enabled after this time, in seconds. This allows more complete charging of batteries when using a constant-current-only charger.
charge_current_thresh	PROD_CHG_CURR_THR	If charging current exceeds this value, the system will consider the battery to be charging.
charge_current_hysteresis	PROD_CHG_CURR_HYST	If charging current falls below (charge_current_thresh – charge_current_hysteresis), the

		system will consider the battery to not be charging.
charge_complete_threshold	PROD_CHG_COMPLETE_THR	If the lowest cell voltage exceeds this voltage when the system transitions from “charging” to “not charging” due to charge current, the system will consider charging to have completed and will reset the state of charge counter.
vmin_sleep	PROD_SLEEP_V	If the lowest cell voltage falls below this voltage, the system will enter sleep mode.
vmin_hibernate	PROD_HIBERNATE_V	If the lowest cell voltage falls below this voltage, the system will enter hibernate mode.
imax_oc	PROD_IMAX_OC	Overcurrent discharge threshold.
imax_sc	PROD_IMAX_SC	Short circuit discharge threshold.
imax_chg	PROD_IMAX_CHG	Overcurrent charge threshold.
overvoltage_delay	PROD_OV_DELAY	Highest cell voltage must exceed vmax_cell for this amount of time (in µs) in order for an overvoltage shutdown to occur. Effective range of this parameter is 1 s to 16 s.
undervoltage_delay	PROD_UV_DELAY	Lowest cell voltage must fall below vmin_cell for this amount of time (in µs) in order for an overvoltage shutdown to occur. Effective range of this parameter is 1s to 8 s.
overcurrent_delay	PROD_OV_DELAY	Discharge current must exceed imax_oc for this amount of time (in µs) in order for an overcurrent shutdown to occur. Effective range of this parameter is 8 ms to 1280 ms.
shortcircuit_delay	PROD_SC_DELAY	Discharge current must exceed imax_sc for this amount of time (in µs) in order for a short circuit shutdown to occur. Effective range of this parameter is 70 µs to 400 µs.
min_fet_switch_interval	PROD_MIN_FET_INT	Cooldown period (in µs) after switching charge or discharge FETs, during which time the charge or discharge FETs will be disabled to limit FET heating.

fet_temp_bitmask	PROD_FET_T_BITS	Bit mask which determines which temperature sensor(s) are assigned to monitoring FET temperatures. Hardware-dependent, should not be changed.
cell_temp_bitmask	PROD_CELL_T_BITS	Bit mask which determines which temperature sensor(s) are assigned to monitoring cell temperatures. Hardware-dependent, should not be changed.
board_temp_bitmask	PROD_BOARD_T_BITS	Bit mask which determines which temperature sensor(s) are assigned to monitoring board temperatures. Hardware-dependent, should not be changed.
internal_thermistor_type	-	Selection for thermistor type for sensors on internal ADCs. Hardware-dependent, should not be changed.
external_thermistor_type	-	Selection for thermistor type for sensors on external ADCs. Hardware-dependent, should not be changed.
has_trickle_charger	PRECHARGE (indirectly)	Indicates whether or not the system has an on-board current-limited charger. If this is 0, the PRECHARGE register will report -1. This is hardware-dependent, but can be enabled or disabled on all current hardware with no side effects.
use_dynamic_i_chg_limit	PROD_DYN_C_LIM_EN	If dynamic charge current limit file is present and valid, setting this value to 1 will enforce the calculated dynamic maximum charge current as a current limit, cutting off the charge FET if the value is exceeded while charging.
use_dynamic_i_dischg_limit	PROD_DYN_D_LIM_EN	If dynamic discharge current limit file is present and valid, setting this value to 1 will enforce the calculated dynamic maximum discharge current as a current limit, cutting off the discharge FET if the value is exceeded while discharging.

has_pt_2		Indicates whether or not the system has a secondary pressure transducer input. Affects which registers are shown in the map.
num_pwm_outputs		Indicates the number of auxiliary PWM output channels the system has. Affects which registers are shown in the map.
num_pwm_inputs		Indicates the number of auxiliary PWM input channels the system has. Affects which registers are shown in the map.
num_extern_adc		Indicates the number of external ADC channels the system has. Affects which registers are shown in the map.
has_sd		Indicates that the system has an SD card slot. Affects which registers are shown in the map.
has_heater		Indicates that the system has an internal pack heater. Affects which registers are shown in the map.
has_xdcr3		Indicates that the system has tertiary transducer present. Affects which registers are shown in the map.

[prdcfg] section

Parameter name	Modbus register name	Description
valid	PROD_VALID (indirectly)	This field serves as an end-of-file marker and a sanity check to protect against truncated files. This parameter should always be the last one in the file, and should always be set to 12345678. If this parameter is not seen, or is set to any other value, the configuration file will be considered invalid. The PROD_VALID register will report 1 when this parameter is correct.

Real-Time Clock

The system contains an onboard real-time clock (RTC) to track the current time. This time value is currently only used to track time elapsed during sleep mode and does not need to be set to the current date and time for correct operation. Its use may be expanded in future firmware revisions.

To set the RTC, write to the RTC register in JAMBUI. The date and time must be entered in the format (YYYY, MM, DD, HH, MM, SS), where HH is a 24-hour time in the range 0-23. Leading zeros must be omitted or the time value may not be interpreted correctly.

Emergency Reset

In the event that the BMS becomes unresponsive, a reset can be forced by supplying a series of timed pulses on the wakeup line. The procedure to do this is as follows:

1. Start with the wakeup line high.
2. Take the wakeup line low for 1 second.
3. Take the wakeup line high for 2 seconds.
4. Take the wakeup line low for 3 seconds.
5. Take the wakeup line high for 5 seconds.
6. Take the wakeup line low. The BMS will reset immediately.

Each step of the reset sequence has a timing tolerance of +/- 950ms. The sequence can be performed by hand or with the wakeup line under the control of another device.

If you make a mistake while entering the sequence, you can immediately restart from the beginning of the sequence.

Data Logging

Beginning with firmware build 7072, the BMS has the ability to capture data logs in response to fault events. The faults that the BMS will respond to can be configured by setting bits in the DATA_LOG_TRIG_MASK register.

The data logging feature is armed as soon as the BMS is powered on. When a rising edge is detected on one of the selected bits in the SYSTEM_FAULT register, the data logger will write a log file containing up to 10 seconds of data leading up to the event, followed by 10 seconds of data after the event. Data in the log files will be captured at 0.25 second intervals. Log files will be saved in CSV format in the *logs* directory in the BMS' file system. A subdirectory for each day will be created in the logs directory, and each log file will be named in the format HHMMSS00.csv, where HH represents hours, MM represents minutes, SS represents seconds, and 00 represents hundredths of seconds. It is recommended to set the BMS' internal clock using the RTC register so that the log file names and internal timestamps will accurately reflect the actual time that events occurred. Assuming the clock remains set correctly, it should not be possible for a new log file to have the same name as an existing file. In the event this does occur, the csv extension on the new log file will be replaced with a number in the range 001 to 999, incrementing sequentially with each new file.

New log files will not be written if there is less than 100KiB of free space remaining on the file system.

If desired, the log function can be triggered for testing purposes by ensuring bit 15 (parameter error) is set in the DATA_LOG_TRIG_MASK register, then writing 0 to the END1 register.

The following values will be recorded as columns in the log file. Unless otherwise noted, data in the log file should correspond directly to data available via Modbus.

TIMESTAMP_UTC – Time stamp of the log entry (Milliseconds since January 1, 1970, local time)
Cell V Min – Lowest cell voltage in the system
Cell V Max – Highest cell voltage in the system
Cell V Raw – List of all cell voltages in the system, unfiltered
Cell V Filt – List of all cell voltages in the system, filtered
Temps – List of all temperature values in the system
Current – Measured battery current
Pack V – Measured overall pack voltage
Balance Bits – List of the balance bits for all cells in the system, formatted as an array of hex values
Int.PT – Internal PT (XDCR) value
Ext.PT – External PT (XDCR2) value
PT Power State – Transducer power state
Stretch – Stretch sensor (XDCR3) value
Chg/Dischg – FET state: PACK_CHG, PACK_CHG_ACTUAL, PACK_DISCHG, PACK_DISCHG_ACTUAL
MONITOR_PASS – The MONITOR_PASS register, formatted as a hex value
MONITOR_FAIL – The MONITOR_FAIL register, formatted as a hex value
Interlock V – The value of the interlock input
Water Alarm – The value of the water alarm(s) in the system
System Faults – The SYSTEM_FAULTS register, formatted as a hex value
Internal State – The INTERNAL_STATE register, formatted as a hex value

Dynamic Current Limiting

Dynamic Charge Limiting

Beginning with firmware build 7130, the BMS has the ability to compute a maximum allowable charge rate and optionally use the computed limit as a safety limit while charging. To use dynamic charge current limiting, a charge limit lookup table file must be created. This file must be in the CSV format, named c_limit.csv, and placed in the cfg directory on the BMS' file system. It must have the following arrangement:

Row 1: Column headers. Allowable headers are OCV, SOC%, and c_rate, which label the open circuit voltage column, state of charge percentage column, and the start of the charge rate limit data, respectively. OCV and c_rate column headings are required. SOC% will be supported in a future firmware release, but is currently ignored.

Row 2: Temperature. Contains temperature values in degrees C for charge rate limit lookup. Temperature values must be sorted in ascending order in this row.

Rows 3+: OCV, SOC%, and charge rate data. Contains the data used for computing charge rate limit. OCV and SOC% data must be sorted in ascending order in their respective columns. The charge rate limit data is specified as a C-rate, not in amps or any other units.

Other than in the header line, all data in the file must be numerical. Any non-numeric characters in the file outside of the header line will cause it to be rejected.

The PROD_DYN_C_VALID register will report 1 if the charge limit lookup table file has been parsed successfully and is considered valid by the BMS.

An example charge limit lookup table file as it might appear in spreadsheet form is shown below:

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1	OCV	c_rate															
2		-30	-25	-20	-15	-10	0	10	20	25	30	35	45	50	55	60	65
3	2.800	0.112	0.085	0.105	0.579	0.611	0.687	1.721	2.635	3.641	3.639	3.594	3.858	3.926	4.416	0.000	0.000
4	2.867	0.069	0.069	0.053	0.550	0.613	0.646	1.630	2.670	3.702	3.618	3.816	3.854	3.692	4.568	0.000	0.000
5	2.933	0.118	0.096	0.067	0.321	0.443	0.731	1.167	2.111	2.960	3.672	3.613	3.909	3.660	4.094	0.000	0.000
6	3.000	0.098	0.083	0.094	0.274	0.446	0.604	1.066	1.675	2.374	2.685	2.972	3.823	3.817	4.362	0.000	0.000
7	3.067	0.063	0.052	0.077	0.252	0.441	0.549	0.930	1.611	2.185	2.462	2.674	3.052	3.108	3.108	0.000	0.000
8	3.133	0.091	0.059	0.124	0.265	0.426	0.458	0.917	1.476	1.867	2.147	2.532	2.734	3.108	3.354	0.000	0.000
9	3.200	0.094	0.084	0.123	0.246	0.342	0.400	0.829	1.293	1.681	2.028	2.236	2.476	2.490	2.771	0.000	0.000
10	3.267	0.100	0.096	0.103	0.242	0.314	0.358	0.712	1.250	1.594	1.702	2.081	2.113	2.529	2.625	0.000	0.000
11	3.333	0.083	0.107	0.099	0.146	0.302	0.366	0.648	1.152	1.338	1.538	1.658	1.917	2.005	2.470	0.000	0.000
12	3.400	0.101	0.088	0.120	0.152	0.270	0.300	0.559	1.026	1.235	1.468	1.542	2.038	1.803	1.836	0.000	0.000
13	3.467	0.069	0.068	0.127	0.177	0.196	0.349	0.534	0.933	1.238	1.306	1.505	1.828	2.029	2.423	0.000	0.000
14	3.533	0.079	0.104	0.051	0.122	0.174	0.277	0.435	0.831	1.015	1.127	1.357	1.698	1.724	1.835	0.000	0.000
15	3.600	0.051	0.089	0.080	0.113	0.219	0.230	0.465	0.646	0.908	1.104	1.344	1.576	1.438	2.170	0.000	0.000
16	3.667	0.090	0.056	0.072	0.082	0.139	0.162	0.306	0.620	0.785	1.010	1.142	1.366	1.208	1.990	0.000	0.000
17	3.733	0.055	0.059	0.087	0.047	0.129	0.200	0.325	0.590	0.639	0.876	1.048	1.035	1.040	1.500	0.000	0.000
18	3.800	0.114	0.116	0.085	0.119	0.180	0.177	0.305	0.563	0.577	0.837	0.852	0.873	1.189	1.432	0.000	0.000
19	3.867	0.089	0.089	0.063	0.074	0.179	0.123	0.243	0.428	0.587	0.815	0.909	0.751	1.066	1.255	0.000	0.000
20	3.933	0.021	0.090	0.062	0.059	0.125	0.182	0.199	0.305	0.452	0.704	0.607	0.568	0.798	0.865	0.000	0.000
21	4.000	0.019	0.072	0.025	0.042	0.096	0.167	0.232	0.237	0.465	0.581	0.463	0.504	0.818	0.854	0.000	0.000
22	4.067	0.034	0.067	0.041	0.127	0.142	0.079	0.139	0.173	0.307	0.289	0.320	0.464	0.406	1.156	0.000	0.000
23	4.133	0.059	0.026	0.091	0.060	0.067	0.098	0.103	0.095	0.162	0.269	0.182	0.477	0.390	0.300	0.000	0.000
24	4.200	0.046	0.077	0.054	0.023	0.130	0.094	0.112	0.167	0.186	0.203	0.225	0.224	0.585	0.417	0.000	0.000

The equivalent data in CSV format would look like this:

```
OCV,c_rate,
,-30,-25,-20,-15,-10,0,10,20,25,30,35,45,50,55,60,65
2.800,0.112,0.085,0.105,0.579,0.611,0.687,1.721,2.635,3.641,3.639,3.594,3.858,3.926,4.416,0.000,0.000
2.867,0.069,0.069,0.053,0.550,0.613,0.646,1.630,2.670,3.702,3.618,3.816,3.854,3.692,4.568,0.000,0.000
2.933,0.118,0.096,0.067,0.321,0.443,0.731,1.167,2.111,2.960,3.672,3.613,3.909,3.660,4.094,0.000,0.000
3.000,0.098,0.083,0.094,0.274,0.446,0.604,1.066,1.675,2.374,2.685,2.972,3.823,3.817,4.362,0.000,0.000
3.067,0.063,0.052,0.077,0.252,0.441,0.549,0.930,1.611,2.185,2.462,2.674,3.052,3.108,3.108,0.000,0.000
3.133,0.091,0.059,0.124,0.265,0.426,0.458,0.917,1.476,1.867,2.147,2.532,2.734,3.108,3.354,0.000,0.000
3.200,0.094,0.084,0.123,0.246,0.342,0.400,0.829,1.293,1.681,2.028,2.236,2.476,2.490,2.771,0.000,0.000
3.267,0.100,0.096,0.103,0.242,0.314,0.358,0.712,1.250,1.594,1.702,2.081,2.113,2.529,2.625,0.000,0.000
3.333,0.083,0.107,0.099,0.146,0.302,0.366,0.648,1.152,1.338,1.538,1.658,1.917,2.005,2.470,0.000,0.000
3.400,0.101,0.088,0.120,0.152,0.270,0.300,0.559,1.026,1.235,1.468,1.542,2.038,1.803,1.836,0.000,0.000
3.467,0.069,0.068,0.127,0.177,0.196,0.349,0.534,0.933,1.238,1.306,1.505,1.828,2.029,2.423,0.000,0.000
3.533,0.079,0.104,0.051,0.122,0.174,0.277,0.435,0.831,1.015,1.127,1.357,1.698,1.724,1.835,0.000,0.000
3.600,0.051,0.089,0.080,0.113,0.219,0.230,0.465,0.646,0.908,1.104,1.344,1.576,1.438,2.170,0.000,0.000
3.667,0.090,0.056,0.072,0.082,0.139,0.162,0.306,0.620,0.785,1.010,1.142,1.366,1.208,1.990,0.000,0.000
3.733,0.055,0.059,0.087,0.047,0.129,0.200,0.325,0.590,0.639,0.876,1.048,1.035,1.040,1.500,0.000,0.000
3.800,0.114,0.116,0.085,0.119,0.180,0.177,0.305,0.563,0.577,0.837,0.852,0.873,1.189,1.432,0.000,0.000
3.867,0.089,0.089,0.063,0.074,0.179,0.123,0.243,0.428,0.587,0.815,0.909,0.751,1.066,1.255,0.000,0.000
3.933,0.021,0.090,0.062,0.059,0.125,0.182,0.199,0.305,0.452,0.704,0.607,0.568,0.798,0.865,0.000,0.000
4.000,0.019,0.072,0.025,0.042,0.096,0.167,0.232,0.237,0.465,0.581,0.463,0.504,0.818,0.854,0.000,0.000
4.067,0.034,0.067,0.041,0.127,0.142,0.079,0.139,0.173,0.307,0.289,0.320,0.464,0.406,1.156,0.000,0.000
4.133,0.059,0.026,0.091,0.060,0.067,0.098,0.103,0.095,0.162,0.269,0.182,0.477,0.390,0.300,0.000,0.000
4.200,0.046,0.077,0.054,0.023,0.130,0.094,0.112,0.167,0.186,0.203,0.225,0.224,0.585,0.417,0.000,0.000
```

This data will be provided by your cell manufacturer.

When the charge limit lookup table file is present and valid, the BMS will compute a maximum allowable charge rate limit on every cell measurement cycle. The limit is computed by performing a bilinear interpolation on minimum cell voltage, and both minimum and maximum cell temperature, and choosing the lower of the two output values. The resulting calculated C-rate is then multiplied by the battery ampacity configured in the product definition file to provide a charge rate limit in real amps. The calculated value is filtered such that the limit can decrease immediately, but can only increase at a reduced rate. This is intended to reduce the possibility of oscillations in the charge current while still maintaining safety. The resulting value will be reported in the CHG_I_LIMIT_REQ register. If the charge limit lookup table file is missing or invalid, this register will report NaN. If the file is valid, but the current temperature and/or voltage values exceed the ranges specified in the table, 0.0 will be reported. Beginning with firmware build 7153, the value reported by this register will be limited to the value of imax_chg set in the product definition file.

If use_dynamic_i_chg_limit is set in the [batt] section of the product definition file, the computed dynamic charge current limit will be used alongside the static charge current limit (set in the product definition file) as an additional current limit while charging. The charge FET will be cut off if either the static or dynamic limits are exceeded, and will remain latched off until the PACK_CHG register is written. The INTERNAL_STATE register can be inspected to determine which limit caused the charge FET to turn off, if desired.

Dynamic Discharge Limiting

Beginning with firmware build 7148, the BMS has the ability to compute a maximum allowable discharge rate and optionally use the computed limit as a safety limit while discharging. To use dynamic discharge current limiting, a discharge limit lookup table file must be created. This file must be in the CSV format, named d_limit.csv, and placed in the cfg directory on the BMS' file system. It must have the following arrangement:

Row 1: Column headers. The only allowable header is d_rate, which labels the start of the discharge rate limit data. The d_rate column heading is required to be in the file. Additional column headers may be supported in a future firmware release, but are currently ignored.

Row 2: Temperature. Contains temperature values in degrees C for discharge rate limit lookup. Temperature values must be sorted in ascending order in this row.

Rows 3+: Discharge rate data. Contains the data used for computing discharge rate limit. The discharge rate limit data is specified as a C-rate, not in amps or any other units.

Other than in the header line, all data in the file must be numerical. Any non-numeric characters in the file outside of the header line will cause it to be rejected.

The PROD_DYN_D_VALID register will report 1 if the discharge limit lookup table file has been parsed successfully and is considered valid by the BMS.

An example discharge limit lookup table file as it might appear in spreadsheet form is shown below:

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
1	d_rate															
2	**-35**	**-30**	**-25**	**-20**	**-15**	**-10**	**0**	**10**	**20**	**25**	**30**	**35**	**45**	**50**	**55**	**60**
3	0.000	1.376	1.419	1.568	1.858	2.392	2.816	4.026	3.811	4.580	5.129	4.843	4.985	5.402	4.843	0.000
4																
5																

The equivalent data in CSV format would look like this:

```
d_rate

-35,-30,-25,-20,-15,-10,0,10,20,25,30,35,45,50,55,60

0,1.376,1.419,1.568,1.858,2.392,2.816,4.026,3.811,4.580,5.129,4.843,4.985,5.402,4.843,0
```

This data will be provided by your cell manufacturer.

When the discharge limit lookup table file is present and valid, the BMS will compute a maximum allowable discharge rate limit on every cell measurement cycle. The limit is computed by performing a linear interpolation of the discharge rate data on both minimum and maximum cell temperature, and choosing the resulting value which is closer to 0. The resulting calculated C-rate is then multiplied by the battery ampacity configured in the product definition file to provide a discharge rate limit in real amps. The calculated value is filtered such that the limit can decrease (towards 0) immediately, but can only increase at a reduced rate. This is intended to reduce the possibility of oscillations in the discharge current while still maintaining safety. The resulting value will be reported in the DISCHG_I_LIMIT_REQ register. If the discharge limit lookup table file is missing or invalid, this register will report NaN. If the file is valid, but the current temperature values exceed the ranges specified in the table, 0.0 will be reported. The value reported by this register will be limited to the value of imax_oc set in the product definition file.

If use_dynamic_i_dischg_limit is set in the [batt] section of the product definition file, the computed dynamic discharge current limit will be used alongside the static discharge current limit (set in the product definition file) as an additional current limit while charging. The discharge FET will be cut off if either the static or dynamic limits are exceeded, and will remain latched off until the PACK_DISCHG register is written. Automatic retries are not attempted if the discharge FET turns off due to the dynamic discharge current limit. The INTERNAL_STATE register can be inspected to determine which limit caused the discharge FET to turn off, if desired.

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